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TITLE: Processor for a data processing system

Detailed Description Text (8):
The .mu.-word also contains a 6-bit field called the micro branching field (UBF) which designates branch tests to be performed within the processor 12 during a .mu.-cycle. Both the UPF and the UBF fields are coupled to the address and branching circuit 45. Branch tests are utilized to alter the address of the next .mu.-word if certain conditions, specified by the UBF field exist. The contents of certain bit locations in designated registers throughout the processor 12 which have particular significance with respect to the state of the processor are coupled to a logic circuit (not shown), typically a multiplexor, in the address and branching circuit 45. The UBF field, which is coupled to this logic circuit, selects certain of these information bits for logical combination, typically ORing, with the low order bits of the UPF field. If the conditions tested for by the UBF field are present, the UPF field is altered in response thereto, and the result is coupled to the NUA bus 36 for selecting the next .mu.-word.

Detailed Description Text (12):
Four general purpose registers, the emit register 50, the processor status word register (PSW) 52, the floating point status register (FPS) 54, and the program micropointer (UPP) register 56, are used, under the control of the UCON register 42, to store certain information during the execution of the program by the processor 12. For example, the emit register 50 is used to store an entire field in the .mu.-word which may be used as data by the data path 30 at a later time. The bits comprising this field are situated in the same location within the .mu.-word that would ordinarily comprise the datapath function field because, as explained earlier, a datapath function will not be needed in this .mu.-word. The PSW register 52 is used to perform the same function as the status register 59 described in aforementioned U.S. Pat. No. 3,710,324. This register contains such information as the present mode of operation of the processing unit, the previous mode of operation, the priority level at which the processor is operating and the condition codes, all of which are described in U.S. Pat. No. 3,710,324.

Detailed Description Text (13):
The FPS register 54 is utilized to store status information similar to the PSW register 52 when an optional floating point processor is coupled to the processor unit 12 and the UPP register 56 is utilized to track the .mu.-word so that, for example if the microroutine is interrupted, the address of the last .mu.-word before the interruption will be stored therein.

Detailed Description Text (14):
Lastly, the processor control unit 32 in FIG. 1 includes a box multiplexor circuit 58 which is utilized under the control of the UCON register 42 to selectively couple the contents of one of the four status registers 50, 52, 54 and 56, to the Din bus 22. This device, along with the other box multiplexors disposed in the other units of the processor 12, will be described in greater detail hereinafter.

Detailed Description Text (16):
The A and B scratch pads, 60 and 62, have certain storage locations therein

reserved for the general purpose registers described in U.S. Pat. No. 3,710,324. For example, these include a program counter register, which is sequentially incremented to indicate the address of the next general or special instruction which the processor 12 will fetch, interpret and execute and a stack pointer register which points to an address in a section of memory reserved as stacks and where the contents of the program counter register and the FPS Register 52 for various microroutines in the processor control unit 32 may be stored for later reference when the processor 12 is interrupted, for example, by an external peripheral device requesting service therefrom.

Detailed Description Text (50):
Referring now to FIG. 6, logic circuitry which may be incorporated in a unit of the processor 12 such as the processor control unit 32, to decode the select and control fields of the UCON register 42 is depicted. In FIG. 6, the inputs to registers 50, 52, 54 and 56, are shown in greater detail. For example, the FPS 54 and the PSW 52 are comprised of three registers each having an input which is individually controlled by the UCON register 42 via a logic gate. Specifically, the input to registers 52 and 54 are controlled by a multiple-input AND gate. Each of these AND gates (152 through 162) has one input coupled to the select processor control unit bit of the select field of the UCON register 42; a second input individually coupled to a bit in the control field associated with the register or storage device controlled by the AND gate; a third bit coupled to the secondary write bus 166; and a fourth input coupled to one of the clock outputs. The secondary write bus 166 is coupled to the secondary write bit in the bus control field of the .mu.-word as depicted in FIG. 4. Accordingly, if it is desired to load the first register 168 of the PSW 52, then the processor control unit select bit and the associated control bit (bit 170 in FIG. 3), in the UCON register 42 must both have a value binary one and the secondary write bus must be enabled. Thereafter, when the P3 clockpulse is generated, the contents on several conductors of the Dout bus 24 will be loaded into this register 168 of the processor status register 52 through gate 152. As earlier mentioned, it is also possible to simultaneously load the data on the Dout bus 24 into registers in different units by selecting more than one unit in the select field of the UCON 42.

Detailed Description Text (52):
If the contents of one of the status registers in the processor control unit 32 are to be coupled in to the data path 30, the box multiplexor 58 must be conditioned appropriately. The box multiplexor 58 is controlled by a plurality of inputs which include the processor control unit select bit from the select field of the UCON register 42, and a plurality of bits from the control field of the UCON register comprising two fields, an enable field and a status register select field. The status register select field is utilized to control which of the four inputs of the multiplexor is selected for coupling to the Din bus 22. The enable field is used to enable the multiplexor and to select between multiplexors in processor units which have more than one multiplexor. With the appropriate control information coupled to the multiplexor 58, the contents of the desired register, such as processor status register 52, are coupled to the Din bus 22 for writing into the C scratch pad of the data path 30 under the control of the C scratch write bus of the .mu.-word in any .mu.-cycle after the UCON register is loaded.

Detailed Description Text (54):
To illustrate, the contents of a status register selected for coupling to the data path are coupled immediately to the Din bus 22 and remain coupled thereto until the microcontrol register 42 is loaded with a new secondary instruction or unless it is temporarily disabled by the bus control circuits in the bus control unit 26 as will be described more fully hereinafter. The data path is loaded with this information in the next .mu.-cycle in which the C scratch pad write bit is enabled. On the other hand, loading information from the Dout bus 24 into a register such as the PSW 52 is implemented differently since this will not occur until the secondary write bit is enabled in a .mu.-word. Thus, the information necessary to set up the

loading of a status register can be loaded into the UCON register 42 ahead of time since it will have no effect until the logic is enabled by a signal from the secondary right bit in a subsequent .mu.-word.

Detailed Description Text (57):
Since the processor 12 of the preferred embodiment communicates with the peripheral devices coupled to the data bus 20 in the same manner as the processors described in the aforementioned patents, it must be able to interrupt the execution of a routine to service a request from a peripheral device assigned a higher priority than the processor at the time the request is issued. If such a peripheral device issues a bus request (BR) signal indicating a request for service from the processor, the BR signal is coupled to the bus control unit 26 and, after determination of the appropriate priority by the priority control circuit 92, a service register (not shown) within the bus control unit 26 will be loaded indicating that a higher priority peripheral device is seeking service from the processor 12.

Detailed Description Text (60):
The vector, which is now residing in the R.sub.n register of the A scratch pad 60, is an address typically within the external memory 16 whose contents will typically contain the address of the first instruction in the routine which must be executed by the processor 12 to service the peripheral device. In addition to the first address in the routine, the processor usually must be provided with a new processor status word which provides the processor with the necessary mode, condition codes and other information necessary to correctly interpret the general instructions in the routine. As a matter of convention, the PSW for this routine, is stored in the subsequent memory address after the vector address provided by the peripheral device. Therefore, the control store 34 must issue instructions or .mu.-words to obtain the contents of both the vector address and the subsequent address in the external 16 memory. Accordingly, in the next .mu.-cycle, n+2,the bus address register 78 is loaded with the contents of the R.sub.n register of the A scratch pad 60 which contains the vector address. During this .mu.-cycle, the contents of the R.sub.n register are incremented by the ALU 66 and thereafter rewritten back into the R.sub.n register. The .mu.-word will also issue a Data In (DATI) command which will cause the contents in the address specified by the bus address register 78 to be coupled into the processor 12 on to the Din bus 22. Thereafter in the n+3 .mu.-cycle, the control store will issue a .mu.-word which causes the MD register to be written with the data presently on the Din bus. The data is of course the first address of the service routine to be executed and will subsequently be loaded into the program counter (PC) register in the scratch pad registers. The new processor status word will be fetched later on in the microroutine after other preliminary operations are performed.

Detailed Description Text (61):
Since the servicing of the peripheral is an interruption in the normal routine of the program, the processor must have a method of remembering the point in the program where it departed to service the peripheral device. Accordingly, two items (words) of information are required to be stored at this time so that the processor can correctly re-enter the program after completing the service routine. These two words are the address of the next instruction to be executed by the processor prior to the interruption by the service request and which is presently contained in the PC register in the scratch pads and the processor status word associated with the next instruction to be executed prior to interruption of the processor and which is located in the PSW register 52 in the processor control unit 32.

Detailed Description Text (62):
For this purpose of storing this type of information, a group of registers, commonly referred to as a stack, are reserved in the memory buffer unit 28 which are monitored by the stack pointer (SP) register in the scratch pad. Accordingly, the control store, in addition to retrieving the first address of the routine and a

new processor status word must also load into the stack the old program count and the old processor status word. Thus, in the next .mu.-cycle, n+4, the control store issues a .mu.-word which specifies a secondary operation and the UCON register 42 is loaded. As depicted in FIG. 7, the secondary operation specified by this .mu.-word is the selection of the PSW register 52 in the processor control unit 32 for coupling to the Din bus 22. Accordingly, the select field of the UCON register 42 must specify selection of the processor unit 32 (i.e., the processor select bit must have a value of binary 1). In addition, the multiplexor enable field and status register select field in the control field of the UCON register 42 must enable the multiplexor 58 and select the processor status register 52 for coupling to the Din bus 22. It should also be noted at this time that the PSW register 52 has been conditioned in advance by the .mu.-word, to be written or loaded at a later point in the routine with the contents of the new processor status word as will be described in more detail hereinafter.

Detailed Description Text (63):
Returning once again to the routine illustrated in FIG. 7, a .mu.-word is issued from the control store 34 during the next .mu.-cycle, n+5, which causes the bus address register 78 to be loaded with the contents of the R.sub.n register in the scratch pad (which now contains the address of the new processor status word; the contents of the MD register (the new program count) to be transferred into the D register and then into the R.sub.n register of A scratch pad; and finally causes the data on the Din bus (the old PSW) to be transferred into the MD register. Additionally, this .mu.-word specifies a DATI operation which will cause the contents of the address in the bus address register (where the address of the new PSW is located) to be transferred on to the data bus 20 for coupling to the memory 16.

Detailed Description Text (64):
Since the .mu.-word issued by the control store 38 during this .mu.-cycle, n+5, specifies a DATI operation which requires a primary transfer over the Din bus 22, the D-cycle and IN/OUT bits in the bus control field of the .mu.-word will have values of binary 1 and 0 respectively. Thus, as earlier explained, the bus/box control circuitry 88 will issue a box multiplexor disable signal during the next .mu.-cycle, n+6,disabling all box multiplexors in the units of the processor and permitting the new PSW to be transferred into the data path 30 without interference from other sources such as, in this case, box multiplexor 58 which is currently selected and enabled by the UCON control circuit 42. In the next .mu.-cycle, n+6, the .mu.-word selected from control store 38 provides for a transfer of the contents in the MD register (the old processor status word) into the shift register 72 followed by the loading of the MD register with the data on the Din bus 22 which, in this case, is the new processor status word.

Detailed Description Text (65):
At this point in the microroutine, both the new and the old processor status words are stored in scratch pad registers in the data path 30. Before transferring the old processor status word into the stack, the PSW register 52 is loaded with the new processor status word. Accordingly, in the next .mu.-cycle, n+7, the .mu.-word selected from the control store 38 causes the D register to be written with the contents of the MD register (the new processor status word).

Detailed Description Text (66):
The next .mu.-word (n+8) in the microroutine specifies a secondary operation in which the PSW register 52 is loaded with the contents of the D register (ie, the new processor status word). As earlier explained, the selection of the PSW register 52 for receipt of the new processor status word via the Dout bus 24 was provided for when the UCON register 42 was loaded during the n+4 .mu.-cycle. However, this preselection has had no effect until the present .mu.-cycle since the secondary write bit of the intravening .mu.-word has not been enabled. In this .mu.-cycle, n+8, however, the secondary write bit of the .mu.-word bus control field has been

enabled (ie, has a value of binary 1) thereby specifying a transfer from the D register 74 over the Dout bus 24 to the storage location and unit selected by the UCON register 42 which in this case, of course, is the PSW register 52 in the processor control unit 32. Additionally, the D register is loaded with the contents of the shift register 72, (ie, the old processor status word) during this .mu.-cycle.

Detailed Description Text (68):
At this point in the illustration depicted in FIG. 7, the new program count and the new processor status word have been retrieved from the extended memory 16, the old processor status word has been transferred from the PSW register 52 into the data path 30 and the new processor status word has been loaded into the PSW register 52. Therefore, all that remains prior to execution of the service routine, is the transfer of the old processor status word and the old program count into the stack. Accordingly, in the next .mu.-cycle, n+9, the .mu.-word issued by the control store 38 specifies that the contents of the stack pointer register located on the scratch pad, be retrieved, decremented and transferred into the shift register 72. As earlier noted, the stack pointer register monitors all entries to and retrievals from the stack and thus contains the address of the last entry on to the stack. This address then must be decremented to provide the address for the next entry into the stack.

Detailed Description Text (69):
In the next .mu.-cycle, n+10, the contents of the shift register are loaded into the bus address register 78. During this .mu.-cycle, the contents of the shift register (SR) 72 are decremented and returned to the shift register, thereby providing the address for the next entry into the stack. Additionally, a data out (DATO) command is initiated, thereby coupling the contents of the D register 74 (the old processor status word) onto the Dout bus 24 for transfer to the stack.

Detailed Description Text (70):
The transfer of the old processor status word to the address specified in the bus address register 78 is completed during the subsequent .mu.-cycle, n+11, and the contents of the SR 72 are transferred into the SP in the scratch pad. This is followed by a .mu.-word in the n+12 .mu.-cycle under the control of which the contents of the SR 72 are transferred to the bus address register 78 and the contents of the PC register in the scratch pad is transferred into the D register. This .mu.-word also specifies a DATO for coupling the contents of the D register (the old program count) onto the Dout bus 24 for transfer to the stack address in the bus address 78 during the next .mu.-cycle.

Detailed Description Text (71):
In the n+13 .mu.-cycle, the PC register in the scratch pad is loaded with the new program count as illustrated in FIG. 7 by retrieving the contents of the R.sub.n register in the scratch pad, transferring it into the D register 74, and thereafter into the PC register. At this point, the processor 12 is ready to begin execution of the service routine. The address of the first instruction of this routine is stored in the PC register and is loaded into the BA register as shown in the n+14 .mu.-cycle in FIG. 7. The addresses for subsequent instructions will be derived by incrementing the PC as explained in the aforementioned U.S. Patents. After completion of the service routine, the old program count and processor status word will be retrieved from the stack using the address in the stack pointer register in the scratch pad whereupon the processor will continue execution of the interrupted program from the point where the interruption occurred.